2.9 inch Low Temperature E-paper Display Series

GDEH029D56LT

Dalian Good Display Co., Ltd.

Version	Content	Date	Producer
1.0	New release	2018/3/12	
1.1	Modify Reference Circuit	2018/10/30	
1.2	Modify Absolute Maximum Rating Modify Reliability Test	2019/02/21	

CONTENTS

1. General Description

GDEH029D56LT is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.9" active area contains 128×296 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 128×296 pixels display
- High contrast & high reflectance
- Support Partial Refresh
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

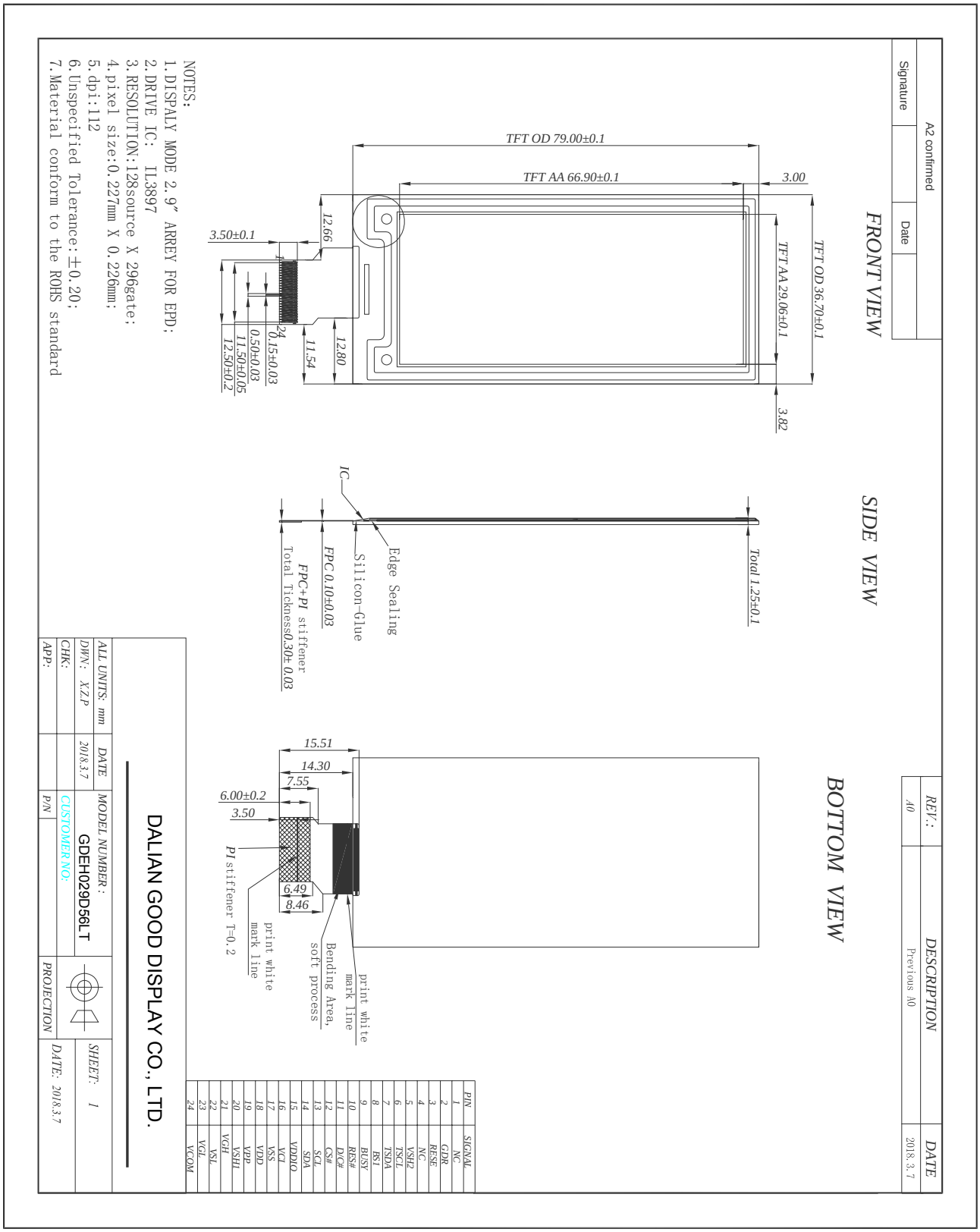
3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128(H)×296(V)	Pixel	Dpi:112
Active Area	29.06(H)×66.90(V)	mm	
Pixel Pitch	0.226×0.227	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0 (V) ×1.25(D)	mm	
Weight	6.5±0.2	g	

5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins e	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.
Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.

7. MCU Interface

7.1 MCU interface selection

The GDEH029D56LT can support 3-wire/4-wire serial peripheral interface. In the Module, the MCU interface is pin selectable by BS1 pins shown in.

Table 7-1: MCU interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

7.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in Figue 7-2.

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:
(1) L is connected to VSS and H is connected to VDDIO
(2) ↑ stands for rising edge of signal

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

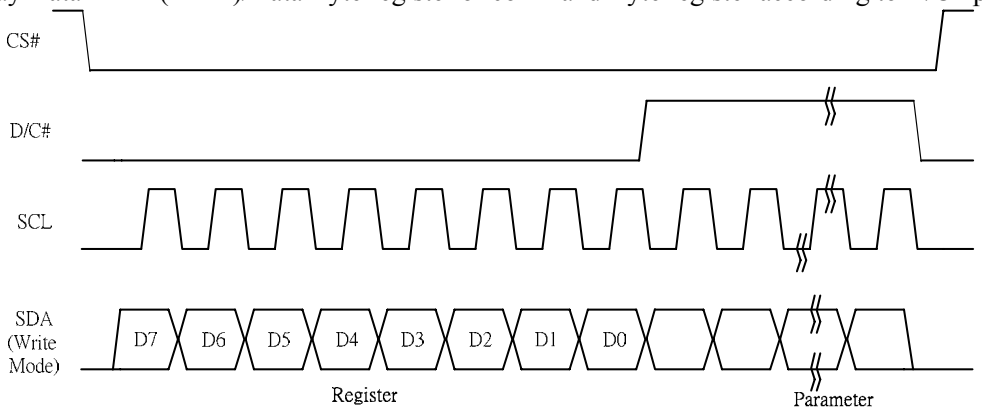


Figure 7-2: Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

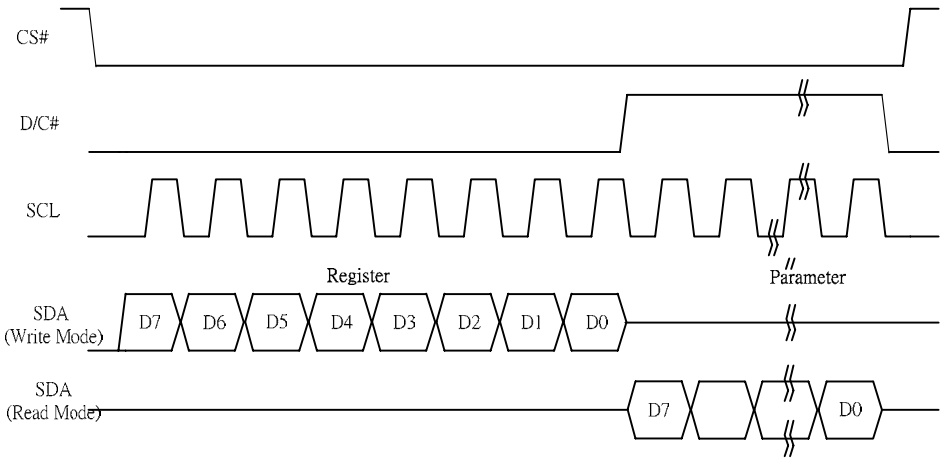


Figure 7-2: Read procedure in 4-wire SPI mode

7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:
(1)L is connected to V_{SS} and H is connected to V_{DDIO}
(2)↑ stands for rising edge of signal

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. shows the write procedure in 3-wire SPI

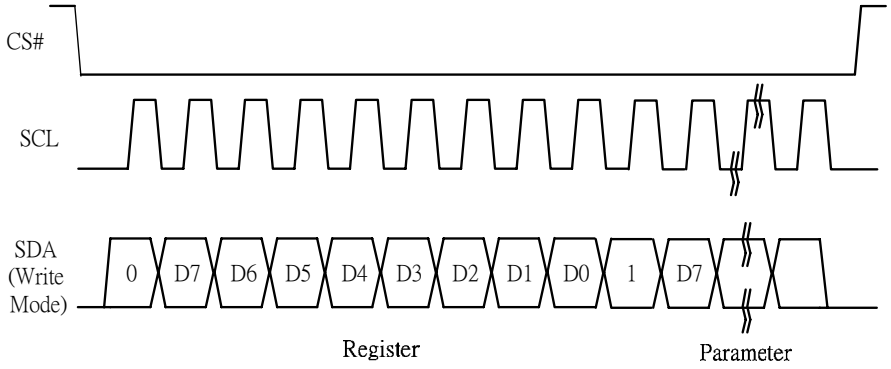


Figure 7-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C#=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0.
4. D/C#=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

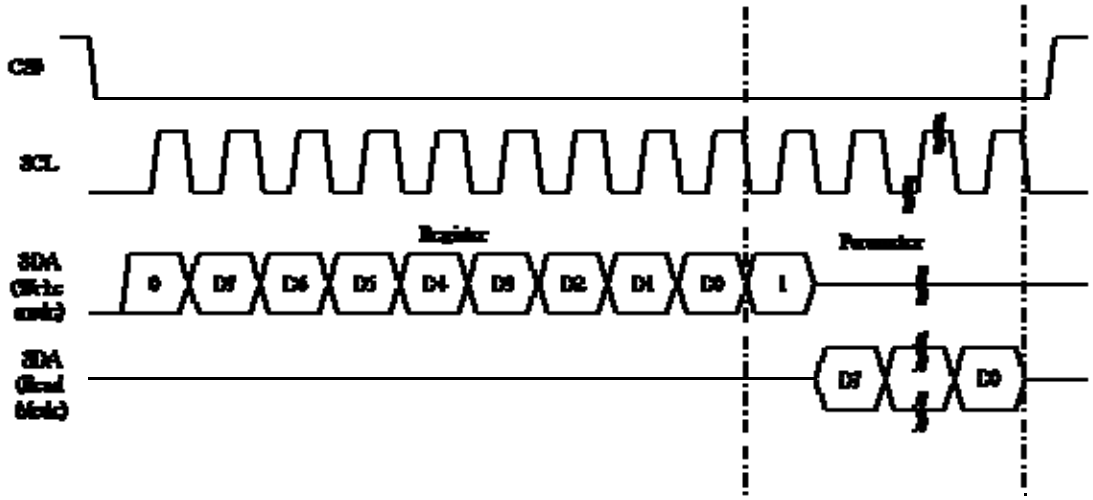


Figure 7-3: Read procedure in 3-wire SPI mode

8. Temperature sensor operation

Following is the way of how to sense the ambient temperature of the module. First, use an external temperature sensor to get the temperature value and converted it into HEX format with below mapping table, then send command 0x1A with the HEX temperature value to the module thru the SPI interface.

The temperature value to HEX conversion is as follow:

1. If the Temperature value MSByte bit D11 = 0, then

   The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then

   The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

9. COMMAND TABLE

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output Control	Set the number of gate. Setting for 296 gates is: Set A[8:0] = 127h Set B[7:0] = 00h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	0	0	0	0	0	0	0	A8		
0	1	-	0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving Voltage Control	Set Gate driving voltage. A[4:0] = 15h [POR], VGH at 19V
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage. A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V C[7:0] = 32h [POR], VSL at -15V
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
			B7	B6	B5	B4	B3	B2	B1	B0		
			C7	C6	C5	C4	C3	C2	C1	C0		
0	0	0C	0	0	0	0	1	1	0	0	Softstart Control	Set Softstart control. A[7:0] = 8Eh B[7:0] = 8Ch C[7:0] = 86h D[7:0] = 3Fh
0	1		1	A6	A5	A4	A3	A2	A1	A0		
0	1		1	B6	B5	B4	B3	B2	B1	B0		
0	1		1	C6	C5	C4	C3	C2	C1	C0		
0	1		0	0	D5	D4	D3	D2	D1	D0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep Mode	Deep Sleep mode Control
0	1	-	0	0	0	0	0	0	A1	A0		A[1:0] Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode1 11 Enter Deep Sleep Mode2
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence. A[2:0] = 3h [POR], A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data is written to the RAM. When AM= 0, the address counter is updated in the X direction. [POR] When AM = 1, the address counter is updated in the Y direction.
0	1	-	0	0	0	0	0	A2	A1	A0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>15</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">VCI Detection</td><td rowspan="2">A[2:0] = 100 [POR] , Detect level at 2.3V
A[2:0] : VCI level Detect
<table><tr><th>A[2:0]</th><th>VCI level</th></tr><tr><td>011</td><td>2.2V</td></tr><tr><td>100</td><td>2.3V</td></tr><tr><td>101</td><td>2.4V</td></tr><tr><td>110</td><td>2.5V</td></tr><tr><td>111</td><td>2.6V</td></tr><tr><td>Other</td><td>NA</td></tr></table>The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.
After this command initiated, VCI detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Temperature sensor control</td><td>Temperature Sensor Selection
A[7:0] = 48h [POR], external temperatrure sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[11:0] =7FFH[POR]</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A11</td><td>A10</td><td>A9</td><td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1B</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="4">Temperature Sensor Control (Read from temperature register)</td><td rowspan="4">Read from temperature register.</td></tr>
<tr><td>0</td><td>0</td><td></td><td>A11</td><td>A10</td><td>A9</td><td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td></td><td></td><td></td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence.

The Display Update Sequence Option is located at R22h
BUSY pad will output high during operation.
User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">RAM content option for Display Update
A[7:0] = 00h [POR]

A[7:4] Red RAM option
<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table>
A[3:0] BW RAM option
<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update Control 2</td><td>Display Update Sequence Option:
Enable the stage for Master Activation
A[7:0]=FFh (POR)
<table><tr><td></td><td>Parameter (in Hex)</td></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then DISPLAY for display mode 1
Then Disable Analog
Then Disable OSC</td><td>C7</td></tr><tr><td><u>Load LUT from OTP</u>
Enable Clock Signal,
Then Load LUT for display mode 1
Then Disable OSC</td><td>91</td></tr><tr><td></td><td></td></tr><tr><td><u>Load TS and then Load LUT from OTP</u>
Enable Clock Signal,
Then Load TS
Then Load LUT for display mode 1
Then Disable OSC</td><td>B1</td></tr></table>
<table><tr><td></td><td>Parameter (in Hex)</td></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then DISPLAY for display mode 2
Then Disable Analog
Then Disable OSC</td><td>CF</td></tr><tr><td><u>Load LUT from OTP</u>
Enable Clock Signal,
Then Load LUT for display mode 2
Then Disable OSC</td><td>99</td></tr><tr><td></td><td></td></tr><tr><td><u>Load TS and then Load LUT from OTP</u>
Enable Clock Signal,
Then Load TS
Then Load LUT for display mode 2
Then Disable OSC</td><td>B9</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM(BW)</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
For Write pixel:
Content of Write RAM(BW)=1
For Black pixel:
Content of Write RAM(BW)=0</td></tr>
<tr><td>0</td><td>0</td><td>26</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Write RAM(RED)</td><td>After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.
For Red pixel:
Content of Write RAM(RED)=1
For non-Red pixel[Black or White]:
Content of Write RAM(RED)=0</td></tr>
<tr><td>0</td><td>0</td><td>27</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Read RAM</td><td>After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly.
The 1st byte of data read is dummy data.</td></tr>
</table>

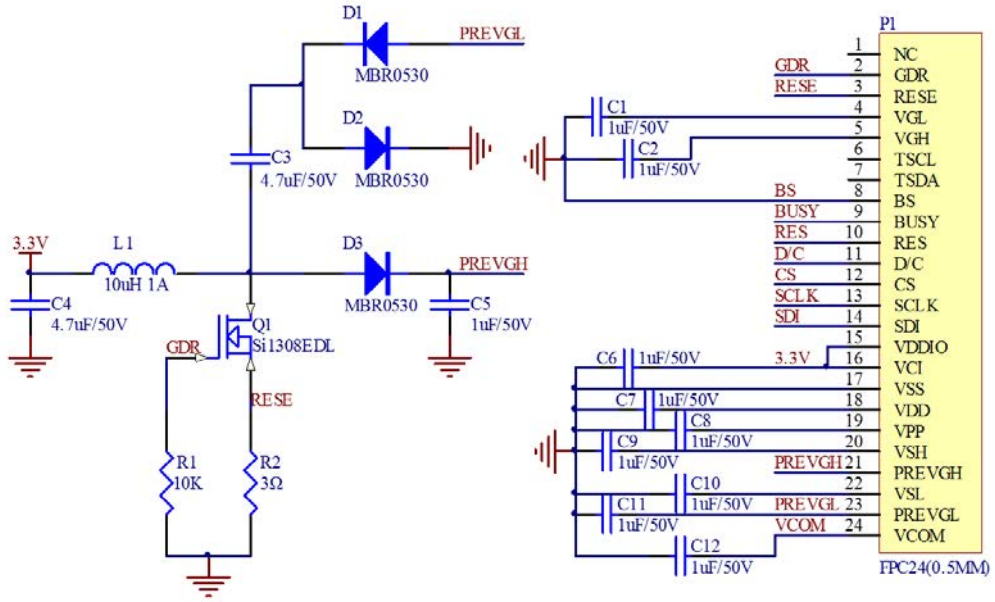
<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>2B</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="3">ACVCOM setting</td><td rowspan="3">Set following values when ACVCOM is used, it will not affect DCVCOM
A[7:0] = 04h
B[7:0] = 63h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Write VCOM register</td><td rowspan="2">Write VCOM register from MCU interface
A[7:0]=00h[POR]
<table>
<tr><th>A[7:0]</th><th>VCOM (V)</th><th>A[7:0]</th><th>VCOM (V)</th></tr>
<tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr>
<tr><td>0Bh</td><td>-0.3</td><td>48h</td><td>-1.8</td></tr>
<tr><td>10h</td><td>-0.4</td><td>4Bh</td><td>-1.9</td></tr>
<tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr>
<tr><td>17h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr>
<tr><td>1Bh</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr>
<tr><td>20h</td><td>-0.8</td><td>5Bh</td><td>-2.3</td></tr>
<tr><td>24h</td><td>-0.9</td><td>5Fh</td><td>-2.4</td></tr>
<tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr>
<tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr>
<tr><td>2Fh</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr>
<tr><td>34h</td><td>-1.3</td><td>6Fh</td><td>-2.8</td></tr>
<tr><td>37h</td><td>-1.4</td><td>73h</td><td>-2.9</td></tr>
<tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr>
<tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>2D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="4">OTP Register Read</td><td rowspan="4">Read Register stored in OTP:
1. A[7:0]~ B[7:0]: VCOM Information
2. C[7:0]~F[7:0]: Display Mode
3. G[7:0]~H[7:0]: Module ID/ Waveform Version [2bytes]</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="10">…</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>H7</td><td>H6</td><td>H5</td><td>H4</td><td>H3</td><td>H2</td><td>H1</td><td>H0</td></tr>
<tr><td>0</td><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="3">User ID Read</td><td rowspan="3">Read 10 Byte User ID stored in OTP:
A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="10">…</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>J7</td><td>J6</td><td>J5</td><td>J4</td><td>J3</td><td>J2</td><td>J1</td><td>J0</td></tr>
<tr><td>0</td><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Status Bit Read</td><td rowspan="2">Read IC status Bit [POR 0x21]
A[5]: HV Ready Detection flag [POR=1]
0: Ready
1: Not Ready
A[4]: VCI Detection flag [POR=0]
0: Normal
1: VCI lower than the Detect level
A[3]: [POR=0]
A[2]: Busy flag [POR=0]
0: Normal
1: BUSY
A[1:0]: Chip ID [POR=01]
Remark:
A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="5">Write LUT register</td><td rowspan="5">Write LUT register from MCU interface [70 bytes] (excluding the analog setting and frame setting)</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>0</td><td>0</td><td>36</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Program OTP selection</td><td>Program OTP Selection according to the OTP Selection Control [R38h]

The command required CLKEN=1.
Refer to Register 0x22 for detail.
BUSY pad will output high during operation.</td></tr>
<tr><td>1</td><td>0</td><td>38</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="3">Write Register for User ID</td><td rowspan="3">Write Register for User ID
A[7:0]]~J[7:0]: UserID [10 bytes]</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="10">…</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>J7</td><td>J6</td><td>J5</td><td>J4</td><td>J3</td><td>J2</td><td>J1</td><td>J0</td></tr>
<tr><td>0</td><td>0</td><td>39</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>OTP program mode</td><td>OTP program mode
A[1:0] = 00: Normal Mode [POR]
A[1:0] = 11: Internal generated OTP programming voltage

Remark: User is required to EXACTLY follow the reference code sequences</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Set dummy line period</td><td>Set A[7:0] = 0Fh</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Set Gate line width</td><td>Set A[3:0] = 0Ch</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Border Waveform Control</td><td>Select border waveform for VBD
A [7:6] Select VBD
<table>
<tr><td>A[7:6]</td><td>Select VBD as</td></tr>
<tr><td>00[POR]</td><td>GS Transition Define A[1:0]</td></tr>
<tr><td>01</td><td>Fix Level Define A [5:4]</td></tr>
<tr><td>10</td><td>VCOM</td></tr>
<tr><td>11</td><td>HIZ</td></tr>
</table>
A [5:4] Fix Level Setting for VBD
<table>
<tr><td>A[5:4]</td><td>VBD level</td></tr>
<tr><td>00[POR]</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH1</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11</td><td>VSH2</td></tr>
</table>
A[1:0]) GS Transition setting for VBD
<table>
<tr><td>A[1:0]</td><td>VBD Transition</td></tr>
<tr><td>00 [POR]</td><td>LUT0</td></tr>
<tr><td>01</td><td>LUT1</td></tr>
<tr><td>10</td><td>LUT2</td></tr>
<tr><td>11</td><td>LUT3</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>41</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Read RAM Option</td><td>Read RAM Option
A[0]= 0 [POR]
0 : Read RAM corresponding to 24h
1 : Read RAM corresponding to 26h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Set RAM X - address Start / End position</td><td>Specify the start/end positions of the window address in the X direction by an address unit
A[5:0] = 00h
B[5:0] = 0Fh</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Set Ram Y- address Start / End position</td><td>Specify the start/end positions of the window address in the Y direction by an address unit
A[8:0] = 127h
B[8:0] = 000h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Set RAM X - address counter</td><td>Make initial settings for the RAM X address in the address counter (AC) A[5:0] = 00h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Set RAM Y - address counter</td><td>Make initial settings for the RAM Y address in the address counter (AC) A[8:0] = 127h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>74</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Set Analog Block control</td><td>A[7:0] = 54h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>7E</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Set Digital Block control</td><td>A[7:0] = 3Bh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

10. Reference Circuit



Note >

1. Inductor L1 is wire-wound inductor. There are no special requirements for other parameters.
2. Suggests using Si1304BDL or Si1308EDL TUBE MOS (Q1) , otherwise it may affect the normal boost of the circuit.
3. The default circuit is 4-wire SPI. If the user wants to use 3-wire SPI, the resistor R4 can be removed when users design.
4. Default voltage value of all capacitors is 50V.

11. ABSOLUTE MAXIMUM RATING

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +6.0	V
T_{OPR}	Operation temperature range	-25 to 25	°C
T_{STG}	Storage temperature range	-25 to 60	°C
-	Humidity range	40~70	%RH

***Note: Avoid direct sunlight.**

12.DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25℃.

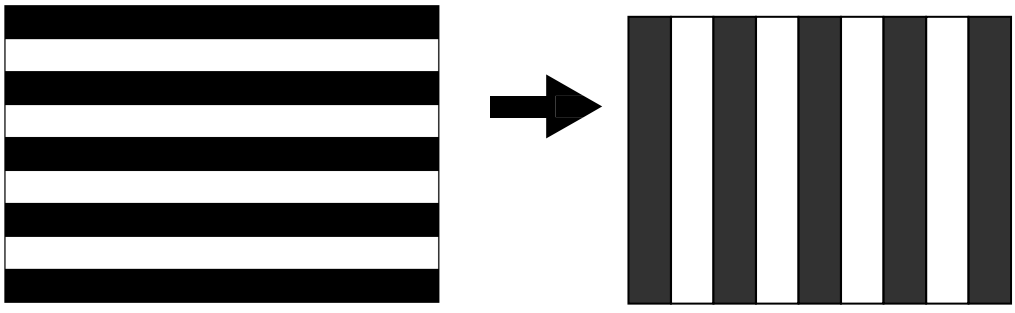
Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	VCI	2.2	3.3	3.7	V
VIH	High level input voltage	-	SDA, SCL, CS#, D/C#, RES#, BS1	0.8VDDIO	-	-	V
VIL	Low level input voltage	-		-	-	0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	BUSY	0.9VDDIO	-	-	V
VOL	Low level output voltage	IOL = 100uA			-	0.1VDDIO	V
Iupdate	Module operating current	-	-	-	8	-	mA
Isleep	Deep sleep mode	VCI=3.3V	--	-	0.6	1	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 12-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by GOOD DISPLAY.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 12-1

The Typical power consumption



13. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.2V to 3.7V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

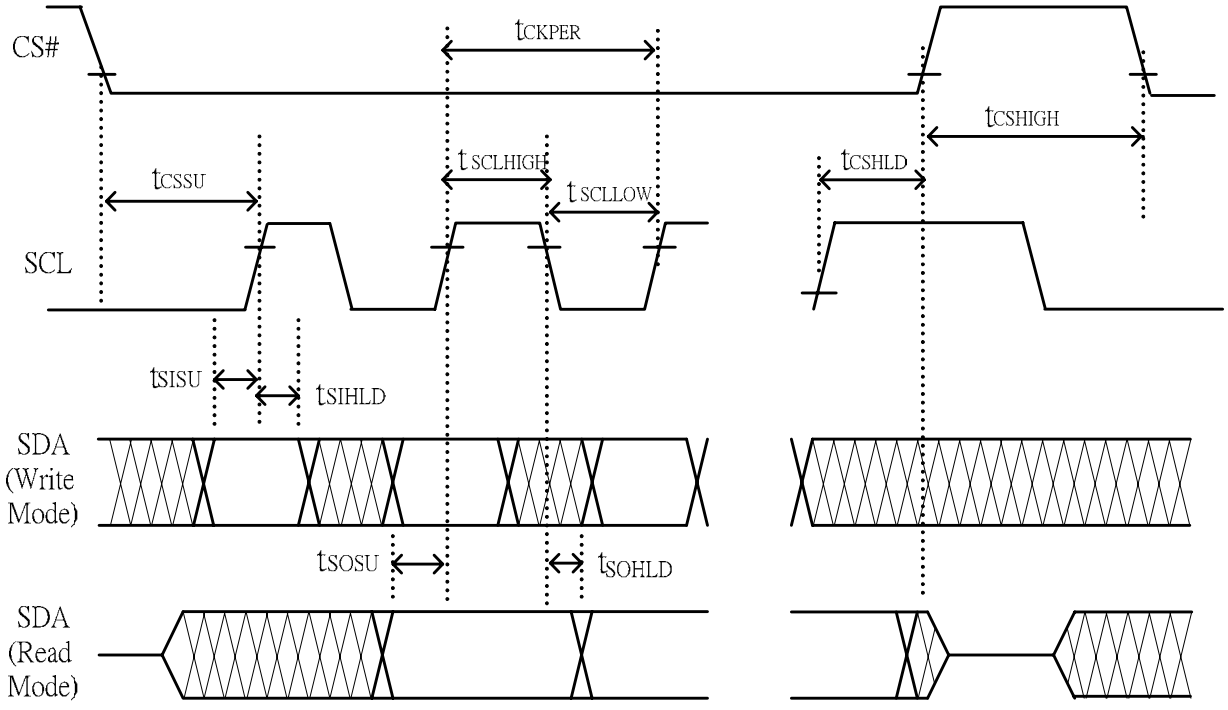


Figure 13-1: Serial peripheral interface characteristics

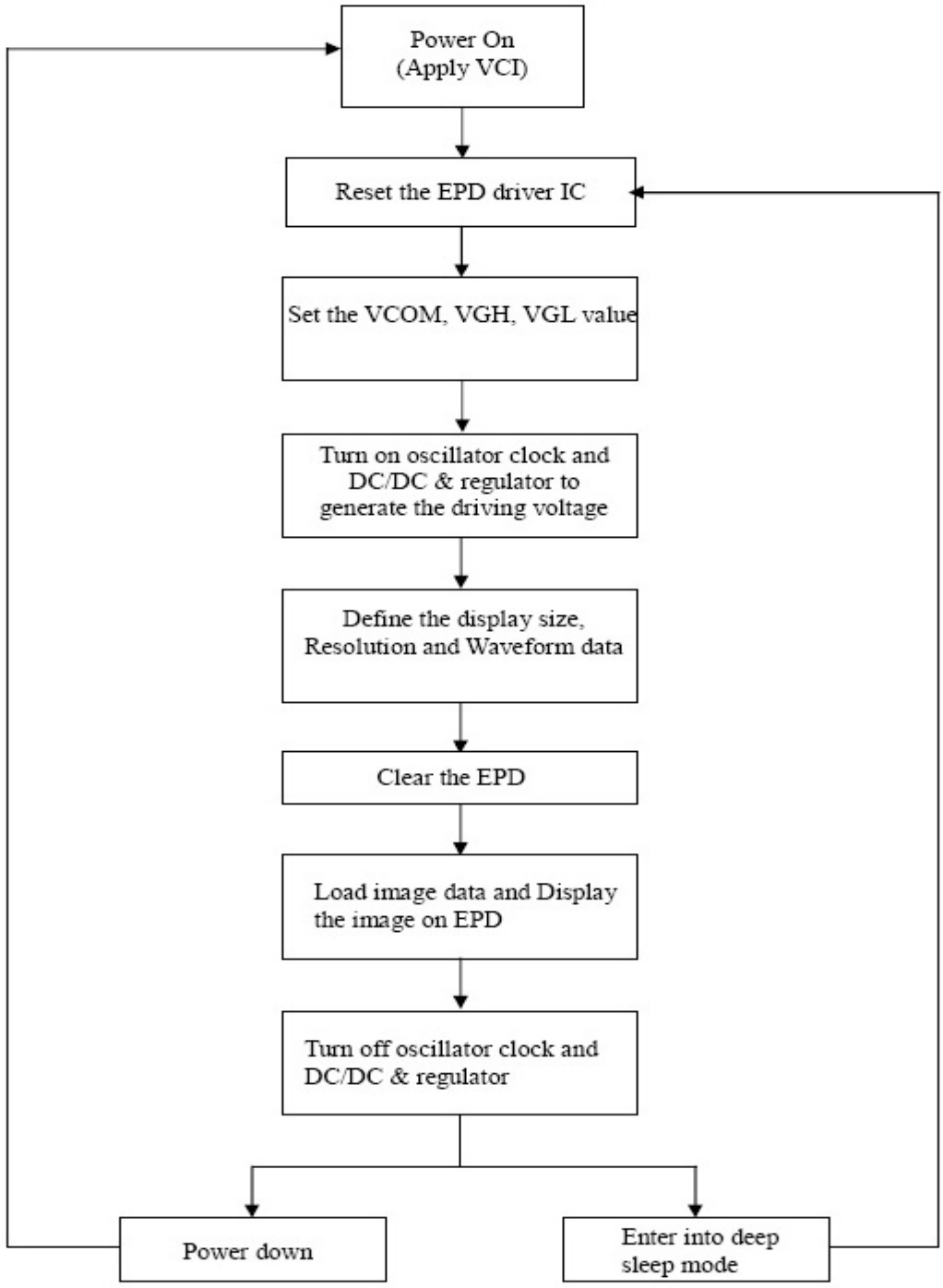
14. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	-25℃	330	-	mAs	-
Deep sleep mode	-	-25℃	0.6	-	uA	-

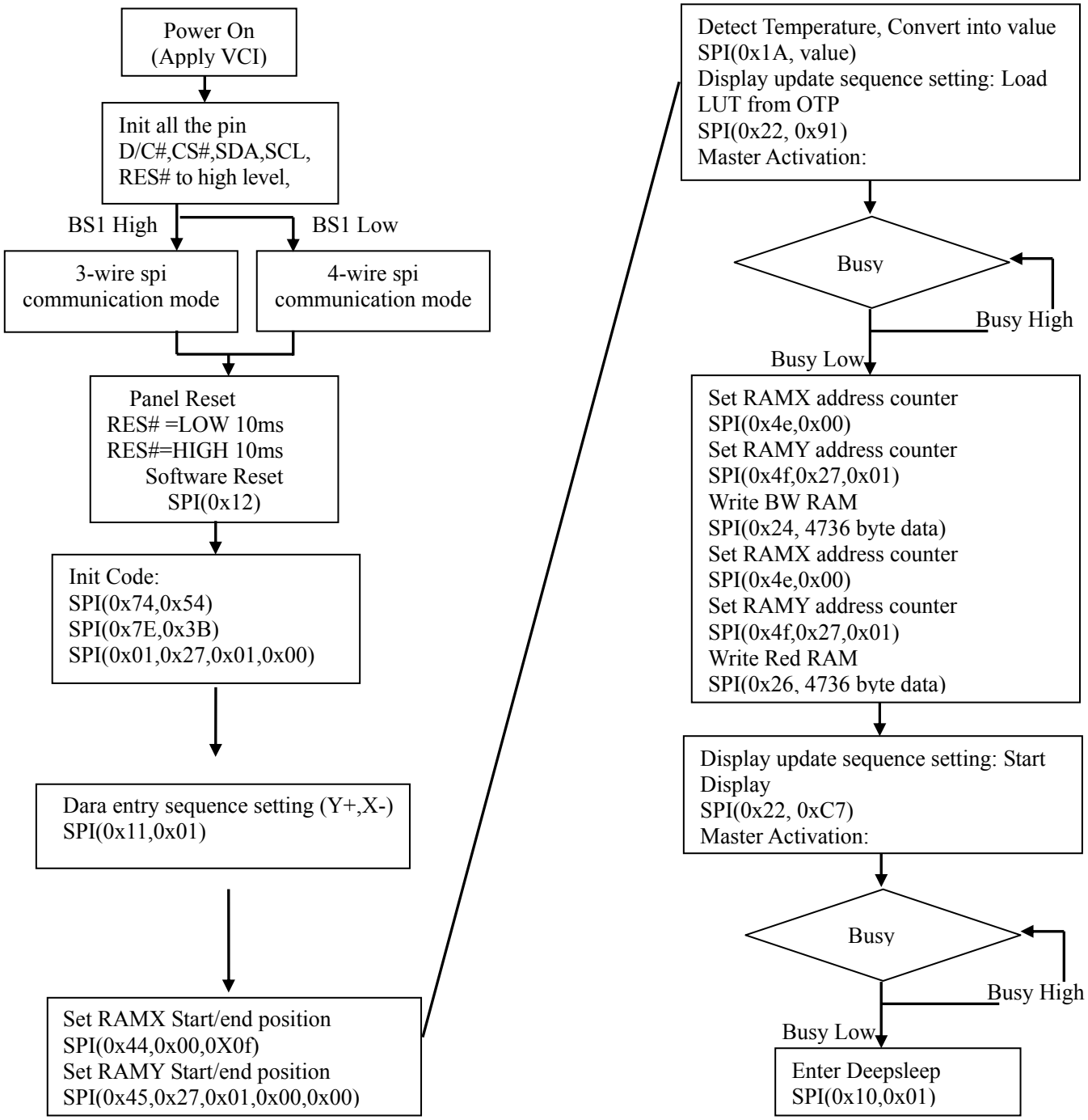
MAs=update average current×update time

15. Typical Operating Sequence

15.1 Normal Operation Flow



15.2 Reference Program Code



16.Optical characteristics

16.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life		- 20℃～50℃		5years or 1000000 times	-	-	Note 16-2

WS: White state, DS : Dark state

m: 2

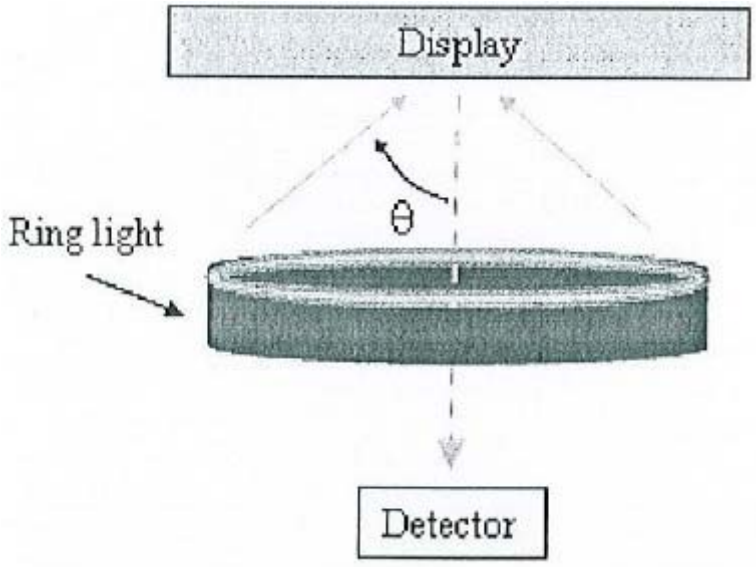
Note 16-1: Luminance meter : Eye - One Pro Spectrophotometer

16.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

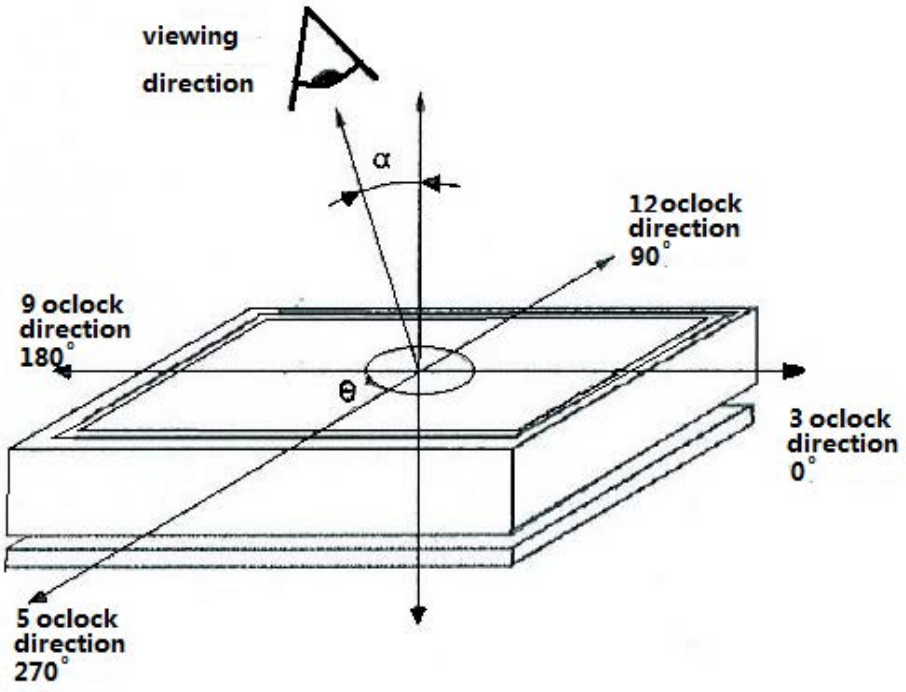


16.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



17. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions	
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.	
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.	
(3) You should adopt radiation structure to satisfy the temperature specification.	
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.	
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)	
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.	
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

18. Reliability test

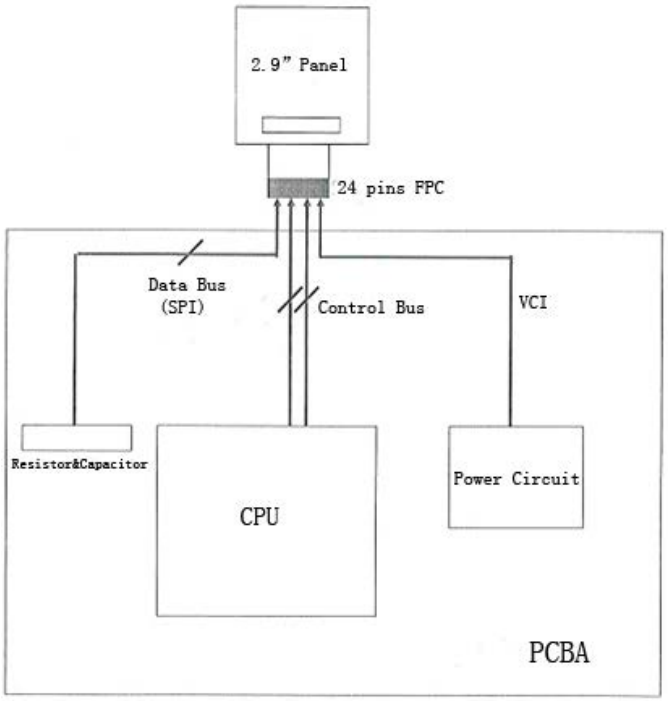
	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=25℃，For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = -25℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=70℃ RH=40%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Storage	T=60℃，RH=80%RH，For 480Hr Test in white pattern	IEC 60 068-2-3CA	
6	Temperature Cycle	-25℃(30min)~60℃(30min)，50 Cycle Test in white pattern	IEC 60 068-2-14NB	
7	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
8	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
9	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	IEC 60068-2-5 Sa	
10	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

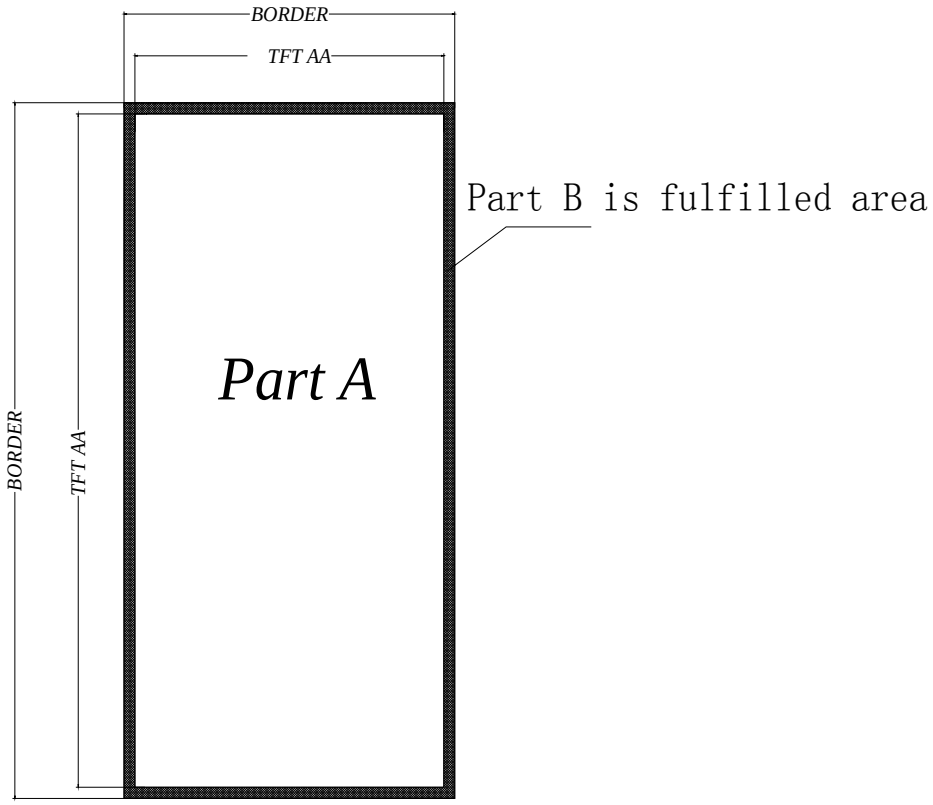
Note1: The protective film must be removed before temperature test.

Note2：Stay white pattern for storage and non-operation test.

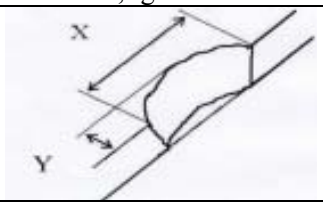
19. Block Diagram

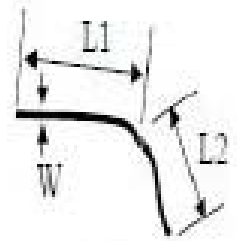


20. PartA/PartB specification

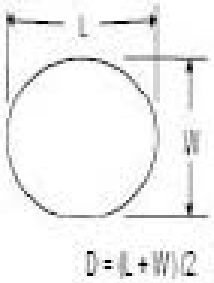


21. Point and line standard

<table>
<tr><th colspan="7">Shipment Inspection Standard</th></tr>
<tr><td colspan="7">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>36.7(H) × 79(V) × 1.25(D)</td><td>Unit：㎜</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td>Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5%RH</td><td>800～1300Lux</td><td>300 ㎜</td><td>35Sec</td><td></td></tr>
<tr><td>Defet type</td><td>Inspection method</td><td colspan="2">Standard</td><td colspan="2">Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td rowspan="3">Electric Display</td><td colspan="2">D≤0.25 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.25 ㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.4 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="2">L≤2 ㎜，W≤0.2 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">2.0mm＜L≤5.0mm，0.2＜W≤0.3mm,</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="2">L＞5 ㎜，W＞0.3 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="2">D≤0.2mm</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.2mm≤D≤0.35mm & N≤4</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.35 mm</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="5">X≤5mm，Y≤0.5mm, Do not affect the electrode circuit , Ignore</td></tr>
<tr><td colspan="5"> 
</td></tr>
<tr><td rowspan="3">Remark</td><td colspan="6">1.Cannot be defect & failure cause by appearance defect；</td></tr>
<tr><td colspan="6">2.Cannot be larger size cause by appearance defect；</td></tr>
<tr><td colspan="6">L=long W=wide D=point size N=Defects NO</td></tr>
</table>



Line Defect



Spot Defect

L=long W=wide D=point size

22. Packing

Packing Spec

Sheet No:

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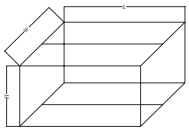
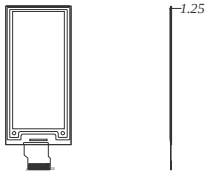
一, Package Type: Box

Box No	GDEH029D56LT
Box size	515*322*170
Containment	240PCS

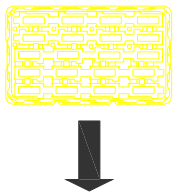


PRODUCT DRAWING

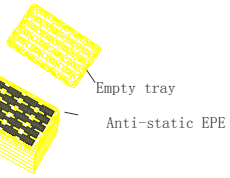


二, Inside package type:Plastic Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	408.86*231.5*2	12 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	20 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

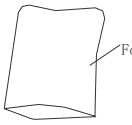


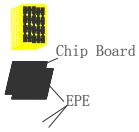
Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.

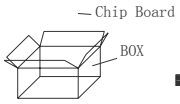


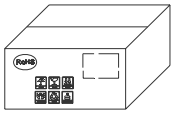
Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 20*12=240 pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:
1) In each case, put 2 bags of desiccant. then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.









Step 4:
1)First put a chip board on the buttom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.

Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign。

Design		Approve		Confirm	
Date		Date		Date	

Packing Spec

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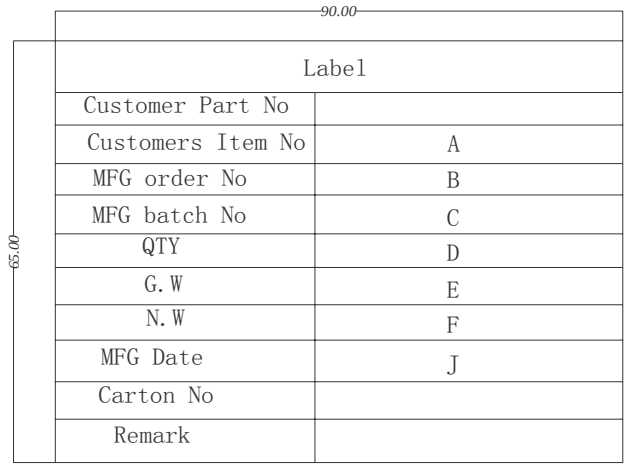
The label outside the carton print as below



Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G.W	E
N.W	F
MFG Date	J
Carton No	
Remark	

NOTE:

1."A" Print customer Item No

2."B" Print customer Order No

3."C" Print MFG Batch No(Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.

4."D"Print product qty

5."E"Print the G.W

6."F"Print the N.W

7."J"Print the MFG date

8.Before packing make sure the FPL batch ,item and qty are the same as which on the Final passed card.

Design		Approve		Confirm	
Date		Date		Date	